REMARKS

The claims are claims 1 to 3, 14 to 18, 24 and 27 to 30.

The application has been amended at many locations to correct minor errors and to present uniform language throughout. The amendments include correction of those errors noted by the Examiner and an update of the status of the co-pending application cited at page 1.

Two new drawing sheets incorporating drawing corrections required by the Examiner are attached.

Claims 1, 2, 15, 16, 17 and 24 are amended. Claims 5 to 13 and 20 to 26 are canceled. New claims 27 to 30 are added. Claims 1 and 15 are amended to include subject matter disclosed in the original application at page 17, lines 1 to 5 and page 20, line 3 to page 21, line 2.

Claims 1 to 26 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner states the term "control word" is indefinite because it neither clearly states it corresponds to a bus width or a fixed bit length nor states it is to be considered a varying bit length.

This rejection is cured by reference to "task attribute bits" a term also used in the original application. The Applicants respectfully submit that one skilled in the art would clearly recognize that this term is confined to no fixed length but can vary with the needs of a particular application. As such this refers to a collection of bits as the Examiner construed "control word" in examining this application.

Claims 1 to 26 were provisionally rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 1-26 of copending U.S. Patent Application Serial No. 09/932,137. The Examiner notes

the application No. 09/932,137 recites "selectively enabled and disabled" and this application recites "configured." The Examiner states that "may be selectively enabled and disabled " is in fact the same as a "may be selectively configured."

Claims 1 and 15 have been amended to recite subject matter not claimed in U.S. Patent Application Serial No. 09/932,137. As amended claims 1 and 15 recite configuration of cache circuitry. This cache configuration operation is not claimed in U.S. Patent Application Serial No. 09/932,137. Accordingly, the provisional double patenting reject should be withdrawn.

Claims 1 to 26 were rejected under 35 U.S.C. 103(a) as made obvious by the combination of Gouzu et al. EP 0 794 481 A2, Gasztonyi U.S. Patent No. 5,339,445, Shaffer et al. U.S. Patent No. 6,298,448 and Gupta et al. U.S. Patent No. 5,996,083.

Claims 1 and 15 recite subject matter not made obvious by the combination of Gouzu et al, Gasztonyi, Shaffer et al and Gupta et al. Claim 1 recites " a memory storing task attribute bits for configuring the cache via the cache configuration circuitry." Similarly, claim 15 recites " configuring the cache circuitry via the cache configuration circuitry to a state responsive to the task attribute bits during execution of said current task." The OFFICE ACTION cites column 5 of Gupta as making obvious control of cache. This portion of Gupta states that the definition of functional units includes cache. However, Gupta fails to teach that this cache is configurable via power control register 106. Accordingly, claims 1 and 11 are allowable over the combination of Gouzu et al, Gasztonyi, Shaffer et al and Gupta et al.

Claims 27 to 30 recite further subject matter not made obvious by the combination of Gouzu et al, Gasztonyi, Shaffer et al and Gupta et al. Claims 27 and 29 each recite that the cache ways are configured via the task attribute bits. None of the cited references include any teaching regarding configuring cache ways.

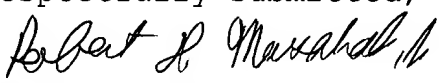
Claims 28 and 39 recite configuring data paths to the cache. None of the cited references include any teaching regarding configuring cache data paths. Accordingly, claims 27 to 30 are allowable over the combination of Gouzu et al, Gasztonyi, Shaffer et al and Gupta et al.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

Texas Instruments Incorporated
P.O. Box 655474 M/S 3999
Dallas, Texas 75265
(972) 917-5290
Fax: (972) 917-4418

Respectfully submitted,



Robert D. Marshall, Jr.
Reg. No. 28,527